In the claims:

1. (Currently Amended) A method comprising:

generating event signals;

storing the event signals in a holding circuit;

producing response signals in a device under test (DUT) in response to the event signals; and

evaluating the DUT based on a comparison of the response signals from the DUT ~~and~~ with the stored event signals received from the holding circuit.

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2. (Original) The method of claim 1 comprising:

generating trigger signals; and

synchronizing each trigger signal with an event signal such that the trigger signal occurs between a rising edge of the event signal and a falling edge of the event signal.

3. (Original) The method of claim 1 comprising:

continuing to store an initial state of each event signal in the holding circuit after transition of the event signal to a subsequent state.

4. (Original) The method of claim 3 comprising:

applying a reset signal to the holding circuit.

5. (Original) The method of claim 1 wherein a minimum width of the event-signal is 25 nano-seconds.

6. (Original) The method of claim 2 wherein a rising-edge of the event-signal is in the range of 45 pico-seconds to 200 pico-seconds.

7. (Original) An apparatus comprising:

a driving circuit including an input and an output;

a first conductor including a first end and a second end;

a first input port for receiving a trigger signal coupled to the input of the driving circuit;

a second input port for receiving an event signal coupled to the first end of the first conductor;

an output port for outputting a hold signal coupled to the second end of the first conductor; and

a second conductor, having an impedance higher than an impedance of the first conductor, and coupled between the output of the driving circuit and a connection point on the first conductor.

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8. (Original) The apparatus of claim 7 wherein the first conductor includes a low impedance microstrip.

9. (Original) The apparatus of claim 7 wherein the second conductor includes a high impedance microstrip having an impedance higher than an impedance of the first conductor.

10. (Original) The apparatus of claim 7, wherein the driving circuit comprises:

a third conductor, having a first end coupled to the first input port for matching the impedance of the trigger signal;

a matching circuit coupled to a second end of the third conductor for matching the level of the trigger signal to the driving circuit;

a sequential logic circuit, having an input coupled to an output of the matching circuit, for holding a signal corresponding to the state of the trigger signal; and

a buffer circuit having an enable input coupled to an output of the sequential logic circuit and having an output coupled to the output of the driving circuit.

11. (Original) The apparatus of claim 10 wherein the third conductor includes a low impedance microstrip.

12. (Original) The apparatus of claim 10 wherein the sequential logic circuit comprises a flip-flop.

13. (Original) The apparatus of claim 10 wherein the buffer circuit comprises a tri-state-buffer.

14. (Original) The apparatus of claim 10 wherein the matching circuit comprises a voltage divider.

15. (Original) The apparatus of claim 10 comprising a reset switch circuit coupled to a reset input of the sequential logic circuit for resetting the output of the sequential logic circuit.

16. (Currently Amended) A system comprising:

a signal source for generating event signals and trigger signals;

a holding circuit for receiving the event signals and trigger signals, and for capturing the event signals;

a device under test (DUT) for producing response signals in response to the event signals; and

a measuring device for evaluating the DUT based on a comparison of the response signals from the DUT ~~and~~ with the captured event signals from the holding circuit.

17. (Original) The system of claim 16 wherein each trigger signal is synchronized with an event signal such that the trigger signal occurs between a rising edge of the event signal and a falling edge of the event signal.

18. (Original) The system of claim 16

wherein the initial state of each event signal is stored in the holding circuit after transition of the event signal to a subsequent state.

19. (Original) The system of claim 16 wherein the holding circuit comprises:

a driving circuit including an input and an output;

a first conductor including a first send and a second end;

a first input port for receiving a trigger signal coupled to the input of the driving circuit;

a second input port for receiving an event signal coupled to the first end of the first conductor;

an output port for outputting a hold signal coupled to the second end of the first conductor; and

a second conductor, having an impedance higher than an impedance of the first conductor, and coupled between the output of the driving circuit and a connection point on the first conductor.

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20. (Original) The system of claim 19 wherein the first conductor includes a low impedance microstrip.

21. (Original) The system of claim 19 wherein the second conductor includes a high impedance microstrip having an impedance greater than an impedance of the first conductor.

22. (Original) The system of claim 19, the driving circuit comprising:

a third conductor, having a first end coupled to the first input port for matching the impedance of the trigger signal;

a matching circuit coupled to a second end of the third conductor for matching the level of the trigger signal to the driving circuit;

a sequential logic circuit, having an input coupled to an output of the matching circuit, for holding a signal corresponding to the state of the trigger signal; and

a buffer circuit having an enable input coupled to an output of the sequential logic circuit and having an output coupled to the output of the driving circuit.

23. (Original) The system of claim 21 wherein the third conductor includes a low impedance microstrip.

24. (Original) The system of claim 21 wherein the sequential logic circuit comprises a flip-flop.

25. (Original) The system of claim 21 wherein the buffer circuit comprises a tri-state-buffer.

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26. (Original) The system of claim 21 wherein the matching circuit comprises a voltage divider.

27. (Original) The system of claim 21 comprising a reset switch circuit coupled to a reset input of the sequential logic circuit for resetting the output of the sequential logic circuit.